Naval Research Laboratory

Washington, DC 20375-5320

NRL/MR/5310--95-7747

Ultrawideband Scanned Array Architecture

T.C. CHESTON
H.P. COLEMAN

SAF, Inc.
Landover, MD

J.B.L. RAO

Radar Analysis Branch
Radar Division

June 30, 1995

Approved for public release; distribution unlimited.

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY (*Leave Blank*)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	June 30, 1995	

4. TITLE AND SUBTITLE

Ultrawideband Scanned Array Architecture

5. FUNDING NUMBERS

PE 62111N
RA11P20

6. AUTHOR(S)

T.C. Cheston,* H.P. Coleman,* and J.B.L. Rao

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

Naval Research Laboratory
Washington, DC 20375-5320

8. PERFORMING ORGANIZATION REPORT NUMBER

NRL/MR/5310–95-7747

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

Office of Naval Research
800 N. Quincy Street
Arlington, VA 22217-5320

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES

*SFA, Inc., Landover, MD 20785

12a. DISTRIBUTION/AVAILABILITY STATEMENT

Approved for public release; distribution unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT (*Maximum 200 words*)

Ultra wideband scanned antenna array architectures are described that make multiple use of switched time-delay circuits to reduce significantly the complexity of time-delay beam steering. A figure of merit is derived comparing the total switchable time-delays with those of a conventional system.

14. SUBJECT TERMS

Wideband, Beam-steering, Phased array, Scanned array, Time-delay, Architectures

15. NUMBER OF PAGES

15

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	SAR

NSN 7540-01-280-5500

Standard Form 298 (Rev. 2-89)
Prescribed by ANSI Std 239-18
298-102

CONTENTS

ULTRA WIDEBAND SCANNED ARRAY ARCHITECTURE

1. INTRODUCTION

Phased arrays are inherently narrow band antennas where the scan angle changes as a function of frequency. This characteristic is exploited in frequency scanned arrays, but with phased arrays it restricts the use of wide instantaneous bandwidth, which is needed to enhance radar capabilities and performance. The narrow bandwidth of phased arrays is due to phase being controlled for the antenna aperture excitation rather than time-delay, and steered beams will scan towards broadside as the frequency is increased, and thus move off the target [1].

For frequency independent steering of the beam, the electrical pathlengths from the feed to each radiating element and from there to the desired equi-phasefront have to be the same. This can be achieved by replacing the phaseshifters (modulo 2π) of a phased array with adjustable time-delay circuits at each element. Unfortunately, this adds greatly to the complexity and cost of the antenna; however, compromises are possible where the array is broken into subarrays with phaseshifters. This approach results in fewer switched time-delay circuits and a corresponding limitation in bandwidth which is reduced to that of the subarray.

With time-delay steering at each radiating element, the only bandwidth limitation is that the spacing between elements should not exceed $\lambda/2$ at the highest frequency to avoid grating lobes. Other restrictions are only those due to components and aperture matching.

The architectures described below give ultrawide bandwidth. They make multiple use of switched time-delay circuits and thereby significantly reduce the total complexity of the system. Various possible methods are discussed, and a figure of merit is derived which is the factor by which the total switchable time-delay of a system is reduced from that of a conventional time-delay system. Making multiple use of switched time-delays introduces losses and is therefore mainly applicable to active arrays, where the losses are compensated by amplification of both transmitter and receiver signals. The methods are applicable to line arrays and, by extension, to two-dimensional arrays.

2. SERIES FEED ARCHITECTURE

Fig. 1 shows the architecture for ultrawideband beamforming with a series feed in its simplest form. Each time-delay circuit shown can give a delay that can be switched to values between 0 and $2d/c$, where d is the inter-element spacing and c the velocity of light. At the highest frequency the elements are spaced by $\lambda/2$ to

Manuscript approved May 15, 1995.

avoid grating lobes, and the delay 2d/c corresponds to 360° of phaseshift, as with a normal phaseshifter. The time-delay circuits are similar to those of a diode phaseshifter with switched line-lengths and are reciprocal so that one setting applies equally for transmitting and receiving. The various lines feeding the elements at the aperture have bias delays making them all equal in length when the time-delays are set to d/c. Therefore, this gives a broadside beam, independent of frequency. The bias delay is about a/2c at the center of the array, where 'a' is the aperture size, and reduces to zero at the edge. It could be provided in stripline taking only little space.

To scan the beam, each one of the time-delay circuits in the right branch of Figure 1 is ideally set to the same value $(d/c)+(d/c)\sin\theta_1$, where θ_1 is the scan angle. Similarly, all the elements on the left are set to $(d/c)-(d/c)\sin\theta_1$. All settings are independent of frequency. This not only gives frequency-independent scanning, but also makes for a very simple scanning calculation with only two drivers necessary if they can handle the power. Under the above conditions, the smallest change in beampointing direction is from changing each one of the switchable time-delays by the smallest bit. With N radiating elements and 'n' bits of delay, the smallest step change in beampointing direction is then $N/2^n$ scanned beamwidths at the highest frequency. For example, when N=64 and n=6 the minimal step change in beam position is one beamwidth. Fine steering (and correction for construction errors) could be added at each module with an additional switched delay, perhaps similar to the branch time-delays. A much simpler (and probably better) solution is to set the branch delays individually and forgo the granular rough- plus- fine steering method discussed above. Each of the branch delays is set to give the closest correct value for that station, that can be achieved with the available number of bits. The most central branch delay circuit is set first, followed sequentially by the more outward circuits, taking into account all previous delay contributions as well as correction data from previous calibration.

A switchable time-delay between 0 and 2d/c, with $d=\lambda/2$ at the highest frequency, gives some excess in available delay, since this value allows scanning to ±90°. Holding scanning to, for example, ±60° requires only .866 times that delay. Additional excess time-delay, if needed, for example, for the correction of construction errors, can be obtained by increasing the time-delay circuit range from a maximum of 2d/c to perhaps 2.2d/c.

Figure 1 shows the central element without a switchable time-delay. Its feed length with bias is the same as that of the other elements with their delay adjusted to d/c. An alternative geometry has two elements in the middle, one each side of the center, and

spaced by d/2 from the center. The time-delay for those two elements would have to be one half of that of the others, i.e. $0.5(d/c)(1\pm\sin\theta_1)$.

For a two-dimensional array, many linear array feed networks like Fig. 1 could be stacked, say in the vertical plane, and combined by one further such network. Monopulse can be added readily with a second vertical combiner and horizontal monopulse outputs. Optimized monopulse outputs with low sidelobes in both sum and difference channels are possible, but require additional complexity.

2.1 Insertion Loss with Series Feed

The major problem with the simple series feed architecture of Fig. 1 is the insertion loss of the time-delay switching circuits. This loss, expressed in dB, is approximately proportional to the number of bits used. The total loss at the end-element is

$$L = n \times L_B \times N/2 \text{ dB}$$

where

(N/2) = Number of radiating elements fed by one branch (The aperture has N or N+1 elements where N is an even number).

n = Number of bits in each switchable branch time-delay circuit.

L_B = Loss per bit in dB.

With practical losses per bit and the large number of bits required for low sidelobes, this loss quickly becomes prohibitive for large antennas. For example, if we assume a loss per bit of $L_B = 0.2$ dB (achieved by Anghel Lab. at S-band)[1] , n=6, and N = 64, then the maximum insertion loss at the edge element is L=38.4 dB. This is probably not acceptable, even in view of a desirable receiver illumination edge taper.

There are methods that can compensate for or reduce the insertion loss. The simplest way is to add two-way amplification in the branch lines at one or more locations, as indicated in Fig. 2, with an appropriate bias-length adjustment.

The insertion loss may actually be reduced by dividing the array into subarrays, each in the form of Fig. 1. The subarrays are then combined by a further, similar, series-feed combiner network. The method is indicated in Fig. 3 which still gives frequency-independent beam steering but at the cost of an increase in the number of time-delay circuits from those shown in Fig. 1.

---

[1] Private communication

With

M = number of subarrays

N_S = number of elements per subarray

n_C = number of bits in the combining (branch) delay network,

the total insertion loss in dB to the last element is

$$L_T = \underbrace{(N_S/2) \times n \times L_B}_{\text{subarray}} + \underbrace{(M/2) \times n_C \times L_B}_{\text{combiner}}.$$

This gives an improvement factor to the loss in dB of

$$(L/L_T) = \frac{N}{N_S + Mn_C/n},$$

where $N = N_S \times M$

When one applies this subarray architecture to the previous example ($N = 64$, $n = 6$) with $M = 8$, $n_c = 9$, and $N_s = 8$, the maximum time-delay is increased from 2d/c to 8x2d/c. Moreover, this architecture yields an improvement factor of $L/L_T = 3.2$ or equivalently, a total insertion loss of 12dB, which should be acceptable.

In all cases, compensation for an appropriate aperture amplitude distribution can be obtained with suitable coupling to the branch line and by adjusting the module amplifier gains [2].

3. CORPORATE FEED ARCHITECTURE

Fig. 4 shows an active parallel or corporate feed architecture with switchable delay-line circuits. In comparison with the series architecture, this parallel feed system requires longer switchable delay-lines. The maximum time-delay required is $Nd/2c = a/2c$. However, there is less insertion loss since only 'm' time-delays are in series where $2^m = N$. The loss is sufficiently small so that it can be compensated by amplification in the solid state modules. For a corporate feed configuration, there is no need for bias time-delay circuits, and monopulse outputs are readily available. The architecture can easily be expanded to a 2-dimensional aperture. The total switchable time-delay required is greater than with the series configuration and smaller than required for a conventional feed with time-delay circuits at each radiating element. This is quantified in Section 5.

4. HYBRID ARCHITECTURE

Combination of corporate and series architectures is possible in a variety of ways, with different parts of the dividing network

using different configurations. Further, the binary divisions of the corporate architecture can be replaced by any multiple division network.

The time-delay architectures can also be combined with phase controlled subarrays. The resultant bandwidth is then that of a subarray. In all cases the switchable time-delays may be increased to allow an excess for error correction.

5. FIGURE-OF-MERIT COMPARISON OF DIFFERENT ARCHITECTURES

A figure of merit (FOM) can be defined which is a measure of the reduction in total time-delay needed by the various feed systems. It is given by the ratio

$$\text{FOM} = \frac{\text{Total switched time-delay for conventional feed system}}{\text{Total switched time-delay for proposed feed system}} .$$

The total switched time-delay is the sum of the maximum values of all switchable time-delay networks used. The conventional system is a configuration where each radiating element has its own unique switchable time-delays. They vary from a/c at the edge to zero at the center, giving a total time-delay of Na/2c.

FOMs for the various configurations discussed are shown in Table 1 and are plotted in Fig. 5. A larger FOM indicates improvement, i.e., smaller total-time delay required by the system.

TABLE 1. COMPARISON OF DIFFERENT ARCHITECTURES

Ultrawideband Architecture	Total Switchable Time-Delay	FOM
Conventional	Na/2c	1
Series feed, Fig. 1	2a/c	N/4
Series subarrays, Fig. 3	4a/c	N/8
Corporate feed, Fig. 4	(a log N)/(c log 2)	0.15 N/(logN)

6. CONCLUSIONS

A number of ultrawideband architectures were described for switchable time-delay beamsteering of an antenna array. The method is akin to the use of tapped delay lines. It uses the same switched time-delay circuits for a multiplicity of antenna elements, and thereby greatly simplifies wideband array scanning in comparison to conventional methods where switchable long time-delay circuits are used at each radiating element.

Series feed networks were found simplest, but with large arrays showed a high insertion loss. The effects of this loss could be reduced by adding amplification. Series feeds with subarrays and corporate feed systems by comparison showed a much smaller insertion loss. However, their total switchable time-delays were greater than with the series configuration, but still much smaller than with a conventional system. A figure of merit was derived, showing the reduction in total switchable time-delay for different architecture when compared with a conventional system.

7. REFERENCES

1. Skolnik, M. I. (ed.), "Radar Handbook", McGraw-Hill Book Co., New York, 1990, Section 7.7.

2. Poirier, J. L., "An Analysis of Simplified Feed Architecture for MMIC T/R Module Arrays", Rome Air Development Center Report RADC-TR-86-236 (AD A185474), February 1989.

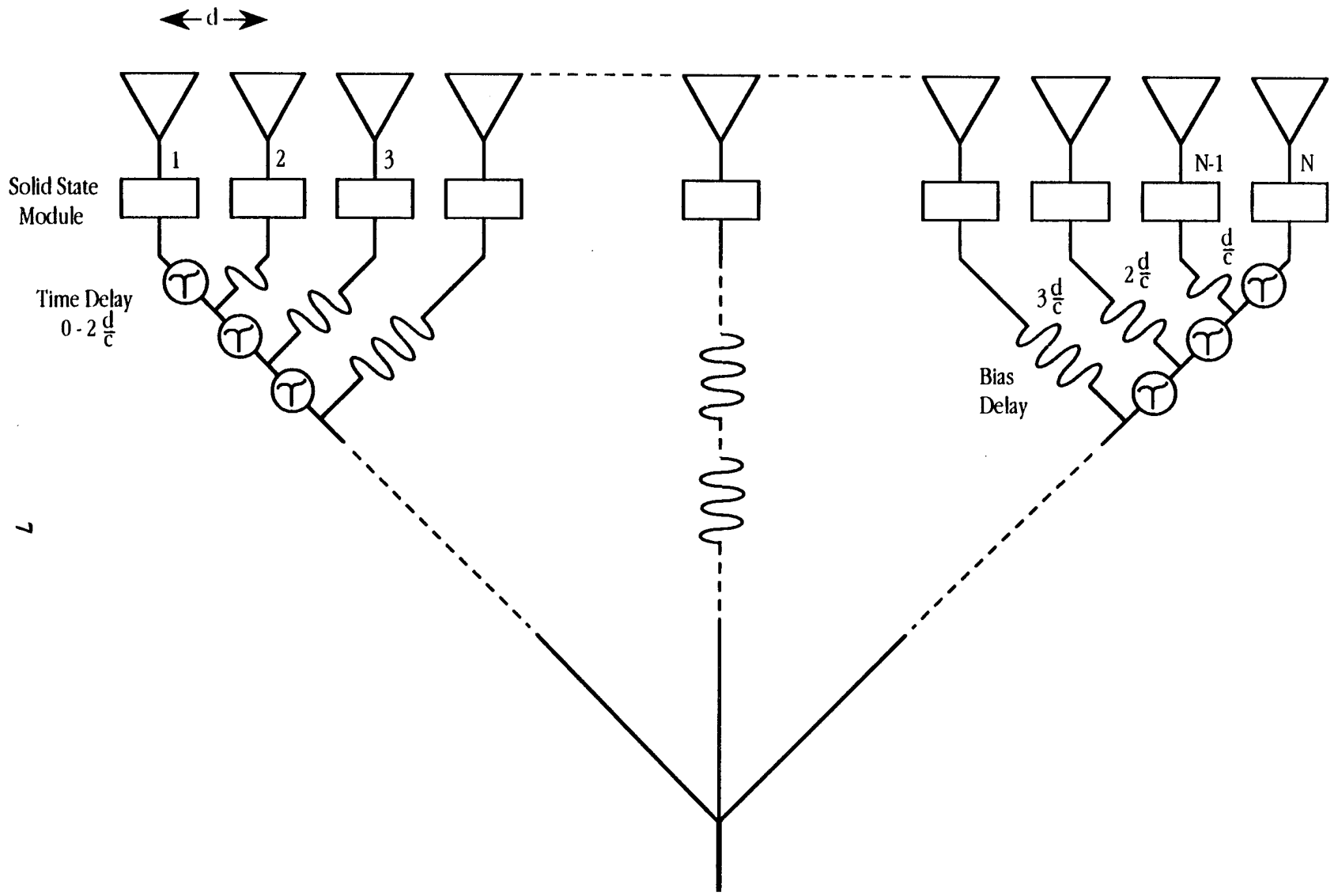

FIG. 1. ULTRA-WIDEBAND SERIES FEED ARCHITECTURE

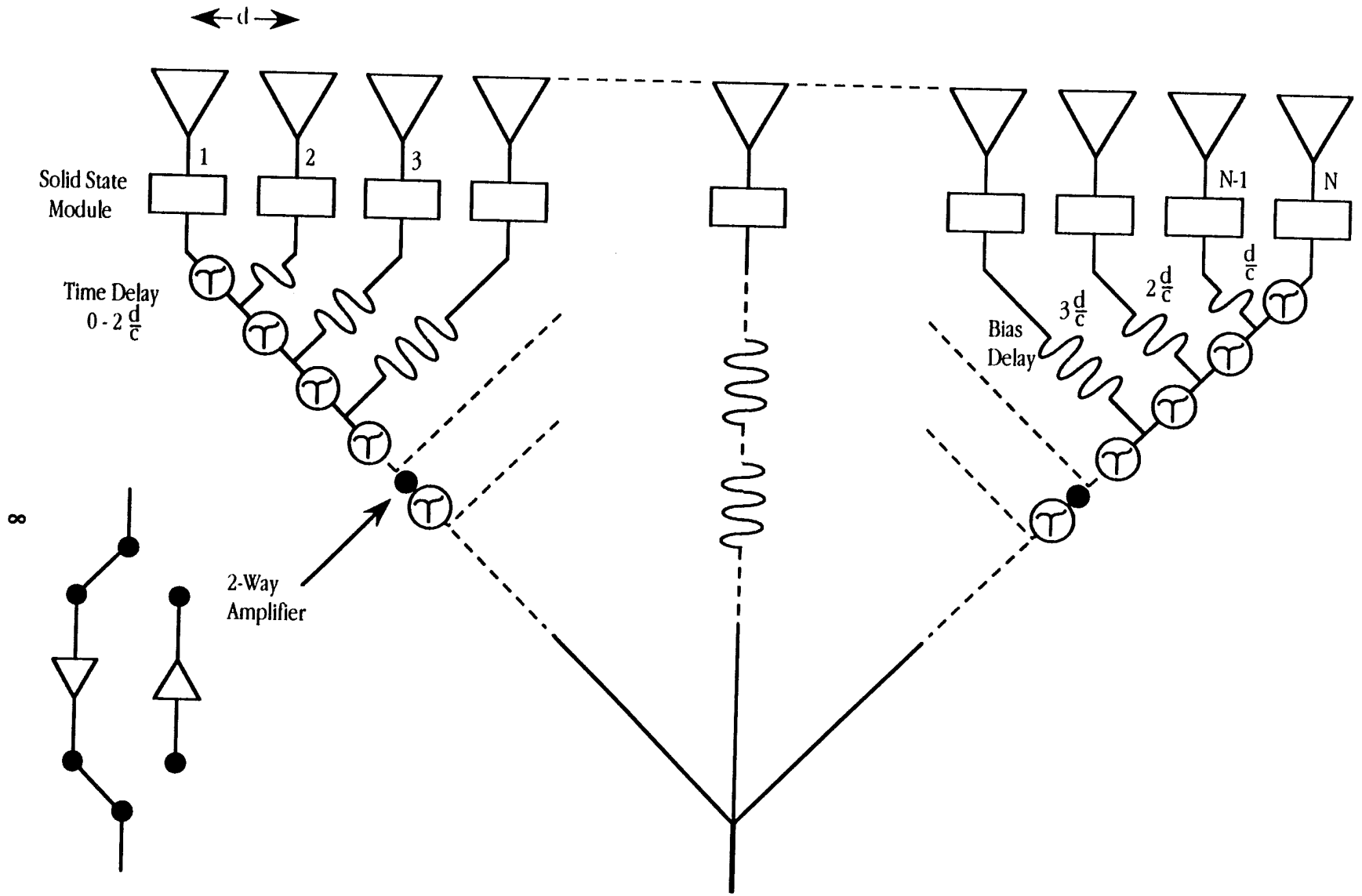

FIG. 2. ULTRA-WIDEBAND SERIES FEED ARCHITECTURE WITH BRANCH AMPLIFIERS

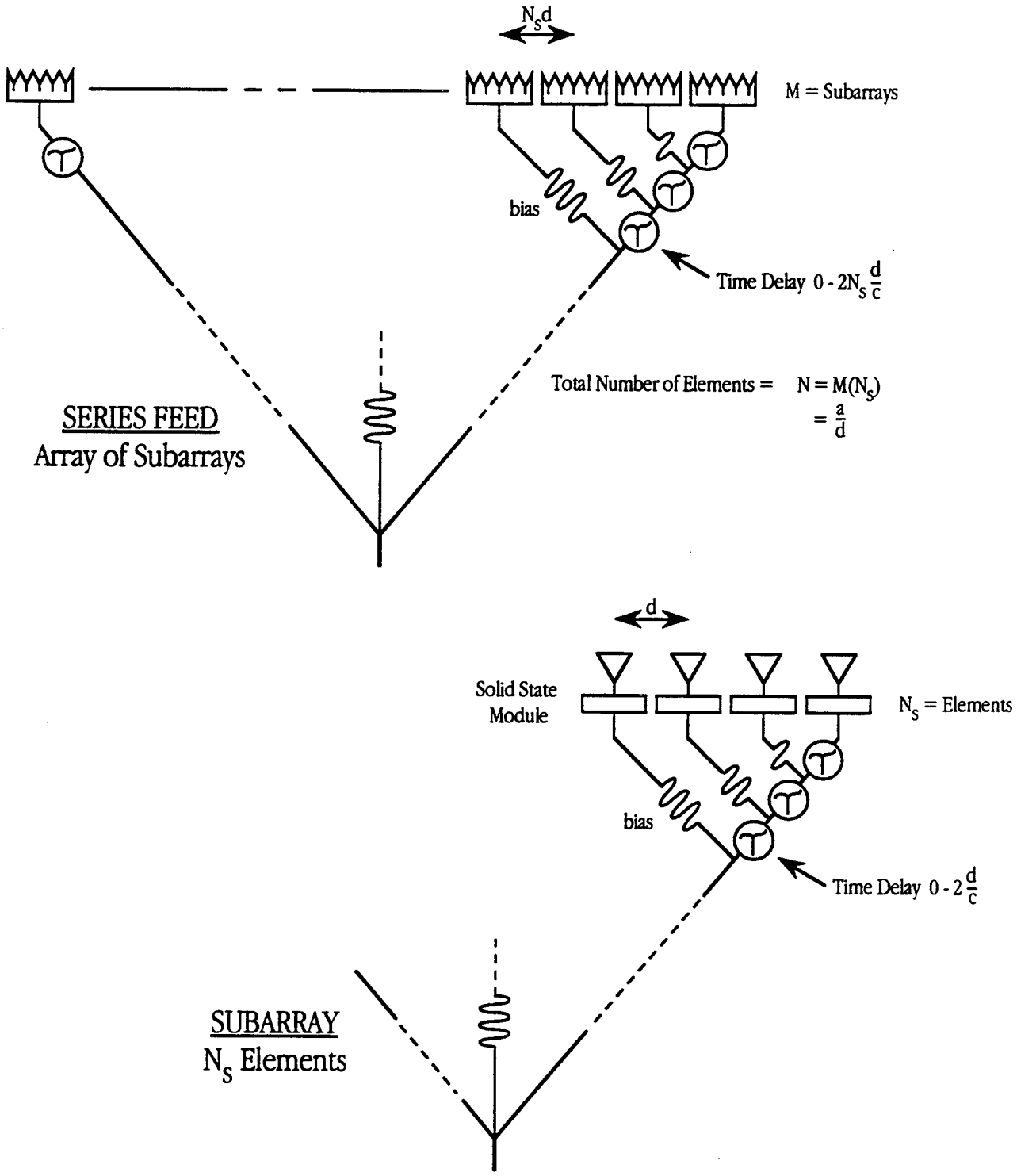

FIG. 3. SERIES FEED ARCHITECTURE WITH SUBARRAYS
total switchable time delay is $4\frac{a}{c}$

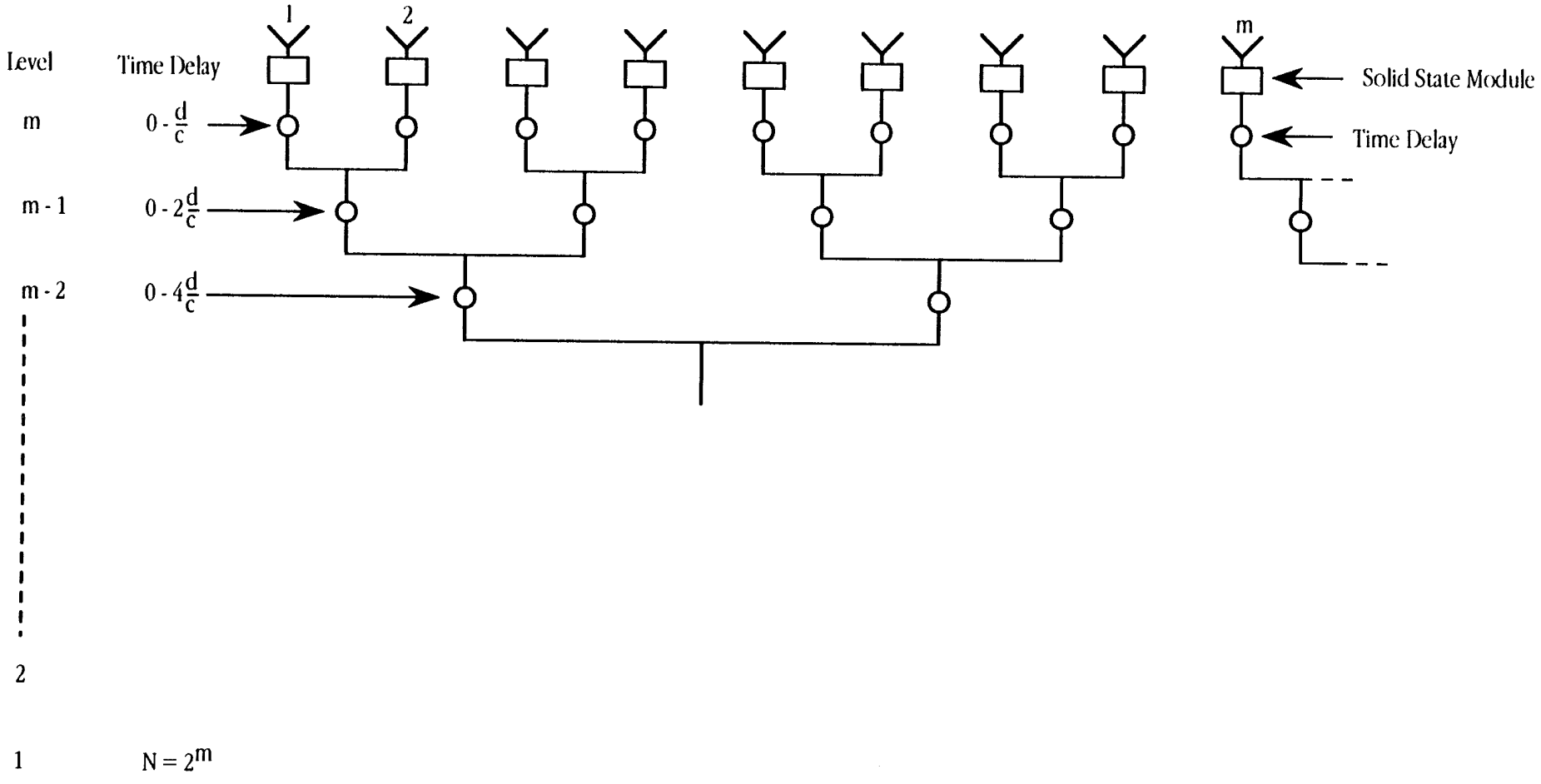

FIG. 4. ULTRA-WIDEBAND CORPORATE FEED ARCHITECTURE

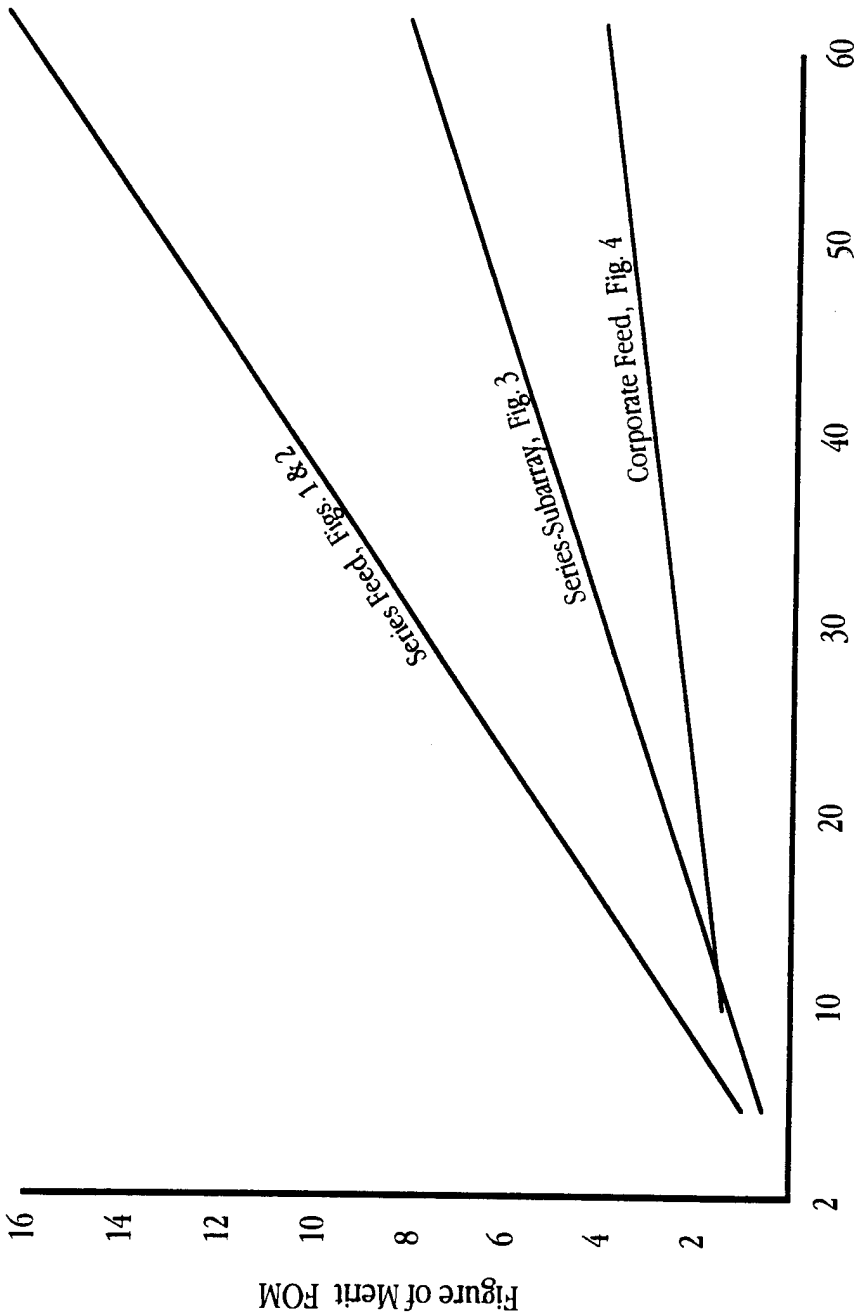

FIG. 5. FIGURE OF MERIT OF DIFFERENT ARCHITECTURES